

In the Claims:

1. (currently amended) A ~~partially fabricated~~ wafer having a probe pad,
comprising:

~~at least one probe pad;~~

multiple test structures ~~which are~~ selectably multiplexed to said probe pad in
dependence on [a] an input voltage applied thereto to said probe pad; and

said probe pad configured also as an output pad from which response of the
selected test structure to the input voltage may be taken.

2. (original) The wafer of Claim 1, wherein said probe pad is located in a scribeline,
and occupies more than half the width of said scribeline.

3. (cancelled)

4. (previously amended) The wafer of Claim 1, wherein said multiple test structures
are selectively multiplexed to said probe pad in dependence on a sequence of voltages
applied to said probe pad.

5-8. (cancelled)

9. (currentlty amended) A scribeline test circuit, comprising:

a test selector circuit located in a single scribeline portion between two adjacent
die locations;

multiple test structures, also located in said single scribeline portion; and

at least one probe pad, also located in said single scribeline portion,
communicable to the multiple test structures;

wherein said test selector circuit makes an electrical connection from said probe pad only to a selected one of said test structures, in dependence on [a] an input voltage applied at said probe pad and from said probe pad response of the selected test structure to the input voltage may be taken.

10. (original) The circuit of Claim 9, wherein said probe pad occupies more than half the width of said scribeline portion.

11. (previously amended) The circuit of Claim 9, wherein said multiple test structures are selectively multiplexed to said probe pad in dependence on the sequence of voltages applied to said probe pad.

12. (currently amended) A method for characterizing integrated circuits using multiple test structure, comprising the steps of:

(a.) applying a ~~selection~~ selecting signal to a probe pad coupled to said multiple test structures[,], to drive a selector circuit to connect a selected one of multiple test structures to said pad; and

(b.) ~~applying a controlled voltage to said pad, and thereby taking measuring~~
measurement of the electrical characteristics of the selected one of said multiple test structures at the probe pad.